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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,397	10/29/2003	Sungju Myoung	Q76047	6800

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,397	MYOUNG ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/29/2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-19 are rejected under U.S.C. 102(e) as being anticipated by Lai et al. (US PGPUB: 2003/0093610 A1)

Claim 1. A flash memory having a map block, the map block comprising: *(Abstract, lines 1-5 – State that there is a flash memory that contains a physical block (a.k.a. map block))*

- a first mapping table containing a physical address allocated to a block of a plurality of blocks, *(Abstract, lines 2-6 – State that there is a mapping table that has physical block addresses)*
- wherein the plurality of blocks constitute a data block and status information of each of the plurality of blocks; *(Section 0022, lines 6-11 – State that "the mapping table 419 includes the address of a corresponding block. Therefore, a mapping table 419 can correspond*

to 128 or less physical blocks. Therefore, the physical blocks can be partitioned into a plurality of segments". This means that there are a plurality of blocks that make up the data block, and there is information on each block)

- a second mapping table containing mapping information between the physical address and a local address of each of the plurality of blocks in the first mapping table *(Section 0024, lines 2-4 – State that the data in the mapping table (a.k.a. local address) can be stored into a partial page of a physical block (a.k.a. physical address), and there is a plurality of blocks)*
- from which error blocks are excluded; *(Section 0023, lines 20-21 – State that the "situation of erroneous connection of data can be effectively reduced", which is like saying that error blocks are excluded)*
- and a third mapping table in which most recent mapping information is written and processed by a specified value to minimize an update operation of the second mapping table. *(Section 0036, lines 1-5 – State that the data (a.k.a mapping information) is written and stored in a "special reserved block of mapping update", which ultimately minimizes the update operation of the second mapping table)*

Claim 2. The flash memory as claimed in claim 1, wherein the map block further comprises a first, a second, and a third spare block for the respective first, second, and third mapping tables. *(Section 0024, lines 10-11 – State that there is a special reserved block for each mapping table)*

Claim 3. The flash memory as claimed in claim 2, wherein the second and third spare blocks store previous mapping information which is updated due to mapping information generated by write and delete operations. *(Section 0024, lines 11-17)*

Claim 4. A flash memory access apparatus, comprising:

- a flash memory including a first mapping table, a second mapping table, a third mapping table and respective first, second, and third spare blocks, *(Section 0022, lines 6-11 – State that "the mapping table 419 includes the address of a corresponding block. Therefore, a mapping table 419 can correspond to 128 or less physical blocks. Therefore, the physical blocks can be partitioned into a plurality of segments". This means that there are a plurality of blocks that make up the data block, and there is information on each block*
- wherein the first mapping table contains a physical address information of a data block, *(Abstract, lines 2-6 – State that there is a mapping table that has physical block addresses)*
- the second mapping table contains mapping information of the first mapping table from which error blocks are excluded, *(Section 0024, lines 2-4 – State that the data in the mapping table (a.k.a. local address) can be stored into a partial page of a physical block (a.k.a. physical address), and there is a plurality of blocks)*
- and the third mapping table contains most recent mapping information; *(Section 0036, lines 1-5 – State that the data (a.k.a mapping information) is written and stored in a "special reserved block of mapping update", which ultimately minimizes the update operation of the second mapping table)*
- and a flash memory controller for generating a fourth mapping table containing free block information through the first, second and third mapping tables obtained from a map block in the flash memory, and for accessing respective physical addresses from and into which data will be read and written by referring to the second and third mapping tables in read operations and the fourth mapping table in write operations. *(Section 0029)*

Claim 5. The flash memory access apparatus as claimed in claim 4, wherein the flash memory controller detects errors due to power cutoff during a data

write process through the fourth mapping table and during a mapping information update process through the second and third mapping tables, and recovers data related to the errors. *(Section 0040 – States that the ECC detects is there has been an abnormal disconnection)*

Claim 6. A method for accessing a flash memory having a first mapping table containing a physical address of a data block read from the flash memory, comprising the steps of:

- receiving a logical address along with a command if read and write operations are requested by a processor; *(Section 0038, line 1 – States that the system obtains the address)*
- checking the logical address in a second mapping table containing mapping information, from which error blocks are excluded, *(Section 0023, lines 20-21 – State that the "situation of erroneous connection of data can be effectively reduced", which is like saying that error blocks are excluded)*
- of physical address information of the data block read from the flash memory and a third mapping table containing the most recent mapping information, in order to perform the read and write operations; *(Section 0024, lines 2-4 – State that the data in the mapping table can be stored into a partial page of a physical block)*
- and accessing the physical address of a specified data block and performing the read and write operations, when the logical address exists within the second and third mapping tables. *(Section 0035 – States that the logical address data is modified and stored)*

Claim 7. The method as claimed in claim 6, further comprising the step of treating the read operation as an error, when the logical address does not exist within the second and third mapping tables. *(Abstract, lines 12-14)*

Claim 8. The method as claimed in claim 6, further comprising the step of accessing a physical address of a free block allocated through a fourth mapping table containing free block information created by a flash

memory controller and performing the write operation, when the logical address does not exist within the second and third mapping tables. *(Section 0030 and 0031 – State that the write operation is performed by accessing a free block of physical memory)*

Claim 9. The method as claimed in claim 6, further comprising the step of initializing the flash memory by loading the mapping information for efficiently accessing the flash memory from a map block of the flash memory according to the operations requested by the processor. *(Section 0038, lines 1-3 – States that the system obtains the address for loading.)*

Claim 10. The method as claimed in claim 6, further comprising the step of detecting errors due to power cutoff occurring during the write operation process and recovering data related to the errors. *(Abstract, lines 12-14)*

Claim 11. The method as claimed in claim 6, wherein the read operation comprises the steps of:

- receiving a given logical address for a data read, if the read operation is requested by the processor; *(Section 0008, lines 6-10 – State that there is a scan (read) action performed upon request by the microprocessor)*
- translating the given logical address into a physical address of the flash memory into which data is written, by referring to the second and third mapping tables; *(Section 0004, lines 5-15 – Describe the process of reading the logical addresses as physical addresses. Section 0005, lines 1-7 – Also describe a similar process))*
- determining in the translation step whether the given logical address is a valid address existing within the data block; *(Section 0040, lines 1-2)*
- and treating the read operation as a read error if the given logical address is not the valid address, or reading data written into the flash memory through the physical address and transmitting the read data to the processor if the given logical address is the valid address. *(Section 0040)*

Claim 12. The method as claimed in claim 6, wherein the write operation comprises the steps of:

- receiving a given logical address for a data write, if the write operation is requested by the processor; *(Section 0028 – States that the system is waiting for a host computer to issue a write instruction)*
- determining whether the given logical address exists within the second and third mapping tables; *(Section 0029, lines 4-5 – State that the system needs to know in which segment the address exists)*
- specifying an arbitrary block specified by a stepwise mapping scheme, if the given logical address exists, or searching for a free block allocated through a fourth mapping table containing free block information created by a flash memory controller as a physical address into which data will be written, if the given logical address does not exist; *(Section 0029 – States that the microprocessor uses the logical block data to find addresses or searching for allocation, writing or mapping)*
- writing the mapping information between the given logical address and the physical address into the third mapping table according to the specified physical address, and changing a pointer of the third mapping table indicating a use region according to the updated mapping information; *(Section 0030, lines 4-5 – State that the data is to be written into a sector buffer, which should rest between the logical and physical addresses. There will inevitably be a pointer or the like to denote which region is being used)*
- receiving data transmitted from the processor in a buffer and writing the input data into the physical address; *(Section 0021, lines 20-22 – State that the physical addresses can be stored in a buffer region. Section 0031, lines 3-6 – State that the data is written directly into the block)*

- determining whether errors have occurred during the data write step; *(Section 0040, lines 1-2)*
- and if errors have occurred according to a result of the determination, writing a block corresponding to the physical address, as an error block, into the first mapping table containing the physical address of the data block read from the flash memory, changing the address information representing current mapping information to an address, *(Section 0040, lines 2-5 – Describe how a block is written upon an error having been occurred)*
- into which the updated first mapping table is written, according to updated error information, and searching the free block to attempt to write the data. *(Section 0041 – States that the information must be retraced and read back into memory)*

Claim 13. The method as claimed in claim 12, further comprising the steps of:

- allocating a new block for updating the mapping information of the third mapping table into the second mapping table and writing the mapping information of the second mapping table updated by the mapping information of the third mapping table into the allocated block, if a storage capacity of the mapping information of the third mapping table allocated to the flash memory is insufficient due to previous mapping information; *(Section 0032 and 0033 – State that a new block is added and new data is written and updated)*
- deleting the previous mapping information written into the third mapping table; *(Section 0034 – States that all data in old block is erased)*
- and changing pointers of the respective second and third mapping tables indicating the use region, according to the mapping information that is updated or deleted. *(Section 0035 – States that the logical address data is modified and stored into a corresponding mapping table)*

Claim 14. The method as claimed in claim 12, further comprising the steps of:

- allocating a new block for updating the mapping information of the third mapping table into the second mapping table and writing the mapping information of the second mapping table updated by the mapping information of the third mapping table into the allocated block, if storage capacities of the mapping information of the second and third mapping tables allocated to the flash memory are insufficient due to previous mapping information; *(Section 0032 and 0033 – State that a new block is added and new data is written and updated)*
- deleting the previous mapping information written into the second and third mapping tables; *(Section 0034 – States that all data in old block is erased)*
- and changing pointers of the respective second and third mapping tables indicating the use region, according to the mapping information that is updated or deleted. *(Section 0035 – States that the logical address data is modified and stored into a corresponding mapping table)*

Claim 15. The method as claimed in claim 12, further comprising the steps of:

- receiving data input from the processor in the buffer and then merging the input data and previously written data to write the merged data into the physical address, if the previously written data exists within the logical address; *(Section 0036 – States that the data is stored into a block of mapping update)*
- and deleting the data in the block into which the data was previously written, after the data write is completed. *(Section 0034 – States that all data in old block is erased)*

Claim 16. The method as claimed in any one of claims 12 to 14, further comprising the step of storing the previous mapping information in second and third spare blocks of the respective second and third mapping tables, whenever

the mapping information of the mapping tables are updated. *(Section 0035 – States that mapping information is stored upon update)*

Claim 17. The method as claimed in claim 9, wherein the step of initializing the flash memory comprises the steps of:

- checking entire information on the flash memory containing stored information related to the first mapping table address information written into the specified block of the flash memory; *(Section 0008, lines 1-4 – State that the whole purpose of this invention is to provide an algorithm that has a lookup table, that will check the information on the flash memory)*
- reading the first mapping table from the map block of the flash memory and reading the second and third mapping tables through respective second and third mapping table regions allocated to the map block; *(Section 0023, lines 13)*
- logically merging the read first, second and third mapping tables to create a fourth mapping table and then storing the created fourth mapping table in a RAM; *(Section 0024 – States that the mapping table can be stored into a physical address block, which resides in the RAM)*
- and waiting to perform the read or write operations requested by the processor. *(Section 0024, lines 1-7 – State that there is a place where the data can be stored while it waiting to perform a function)*

Claim 18. The method as claimed in claim 17, wherein the step of reading the first mapping table comprises the steps of:

- searching for the address information of the first mapping table from the specified block by using the stored information; *(Section 0006, lines 15-16 – State that the microprocessor will scan all addresses. Section 0036, lines 3-5 – State that the data is capable of being searched)*

- detecting the address information and searching the first mapping table from the first mapping table block region allocated to the flash memory so as to write the address information searched in the first mapping table into the specified block, if the address information exists, *(Section 0006, lines 16-22 – State that the addresses will be detected and the information will be written if the address exists)*
- or searching the first mapping table block region so as to generate the first mapping table and then to write the address information generated in the first mapping table into the specified block, if the address information does not exists; *(Abstract, lines 12-14)*
- and reading out the first mapping table from the flash memory by using the searched or generated address information. *(Section 8-10 – States that the microprocessor scans addresses to all physical blocks)*

Claim 19. The method as claimed in claim 10, wherein the step of detecting the errors and recovering the relevant data comprises the steps of:

- checking the second and third mapping tables from the map block of the flash memory to determine whether a plurality of the second and third mapping tables currently used exist within the map block; *(Section 0031, lines 1-3 – State that here is a check of whether or not there are duplicates)*
- if the plurality of second and third mapping tables exist in the map block, determining that the errors have occurred due to power cutoff during the process of updating the mapping information and deleting the most recent mapping information written into the second and third mapping tables; *(Section 0032 – States that the new data is written into clean blocks if the tables are duplicates)*
- merging the checked second and third mapping tables or the second and third mapping table with the most recent mapping information deleted there from and the first mapping table read out from the flash memory, into the fourth mapping table generated by the flash memory

controller during an initialization process of the flash memory; *(Section 0035 – States that the logical address data is modified and stored into their corresponding mapping tables so that relations could be built between them. Building a relation, is like merging the tables)*

- searching a first free block form the merged fourth mapping table and determining whether the searched free block is a pure free block into which no data are written; (*Section 0036, lines 3-5 – State that the data is capable of being searched. Section 0030 – States that the microprocessor figures out which block of data needs to be accessed and utilized)*
- and if the searched free block is not the pure free block, determining that the errors have occurred due to power cutoff during the process of writing the data and deleting the written data. *(Section 0034 – States that the data is deleted after it is written)*

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER